CLAIMS:

1. A divider circuit for reducing anomalous output timing pulses, comprising:

a division selection line;

at least one latch coupled to the division selection line;

a comparator coupled to the division selection line;

an input clock line;

a first synchronizer coupled to the output of the latch;

a frequency divider coupled to the output of the synchronizer and the input clock line; and

a second synchronizer coupled to the output of the first comparator and the output of the frequency divider.

2. The circuit of Claim 1, further comprising:

an OR circuit coupled to the output of the second synchronizer.

3. The circuit of Claim 2, further comprising a delay circuit coupled to the output of the OR circuit.

4. The circuit of Claim 3, further comprising an output of the delay circuit coupled to the reset of the second synchronizer.

5. The circuit of Claim 2, wherein the output of the OR circuit is coupled to the reset of the frequency divider.

6. The circuit of Claim 2, wherein the output of the OR circuit is coupled to the reset of the first synchronizer.

7. The circuit of Claim 2, wherein the output of the OR circuit is coupled to the enable of the latch.

8. The circuit of Claim 2, further comprising an external reset coupled to an input of the OR gate.

9. The circuit of Claim 1, wherein the frequency divider is a pre-existing component.

10. The circuit of Claim 1, wherein at least the frequency divider circuit and the first and second comparators are integrated into the same integrated circuit chip.

11. A computer program product for reducing anomalous timing pulses, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for inputting data over a division selection line, wherein a latch is coupled to the division selection line, and wherein a comparator is coupled to the division selection line and the input clock line;

computer code for inputting data over an input clock line;

computer code for synchronizing the output of the latch;

computer code for frequency dividing the output of the first synchronizer; and

computer code for synchronizing the output of the comparator and the output of the frequency divider.

12. A processor for reducing anomalous timing pulses, the processor including a computer program comprising:

computer code for inputting data over a division selection line, wherein a latch is coupled to the division selection line, and wherein a comparator is coupled to the division selection line and the input clock line;

computer code for inputting data over an input clock line;

computer code for synchronizing the output of the latch;

computer code for frequency dividing the output of the first synchronizer; and

computer code for synchronizing the output of the comparator and the output of the frequency divider.

13. A method of generating glitch-free output, comprising:

receiving a first division selection value into a latch;

receiving a first division selection value into a comparator;

outputting a first value from the latch;

comparing the first division selection value and the first value;

generating a comparison value as a function of the comparison;

synchronizing the comparison value with an output of a divider;

outputting the synchronized comparison value; and

applying a reset value to the latch as a function of the synchronized comparison value; and

applying a reset value to the divider as a function of the synchronized comparison value.

14. The method of Claim 13, further comprising generating a delayed synchronized comparison value.

15. The method of Claim 14, further comprising applying the delayed synchronization comparison value to a reset of a first synchronizer which performs the outputting of the synchronized comparison value.

16. The method of Claim 13, further comprising synchronizing the output of the latch to a timing signal.

17. The method of Claim 16, further comprising employing a second synchronizer for synchronization.

18. The method of Claim 16, further comprising applying the synchronized output of the latch to an input of the divider.

19. The method of Claim 13, further comprising applying the output of the first synchronizer to the reset of a second synchronizer.